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DATA SHEET

BLF175
HF/VHF power MOS transistor

Product specification

September 1992

Philips
Semiconductors

PHILIPS

HF/VHF power MOS transistor BLF175

FEATURES

- High power gain
- Low intermodulation distortion
- Easy power control
- Good thermal stability
- Withstands full load mismatch
- Gold metallization ensures excellent reliability.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the HF/VHF frequency range.

The transistor has a 4-lead, SOT123 flange envelope, with a ceramic cap. All leads are isolated from the flange.

A marking code, showing gate-source voltage (V_{GS}) information is provided for matched pair applications. Refer to the 'General' section for further information.

PINNING - SOT123

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

PIN CONFIGURATION

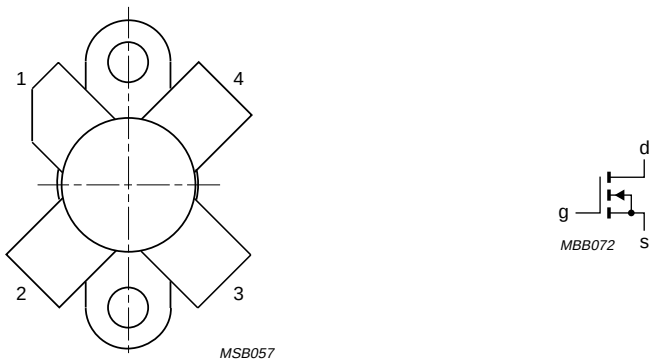


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MH_Z)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_P (dB)	η_D (%)	d_3 (dB)
class-A	28	50	800	8 (PEP)	> 24	–	< –40
class-AB	28	50	150	30 (PEP)	typ. 24	typ. 40 (note 1)	typ. –35
CW, class-B	108	50	30	30	typ. 20	typ. 65	–

Note

1. 2-tone efficiency.

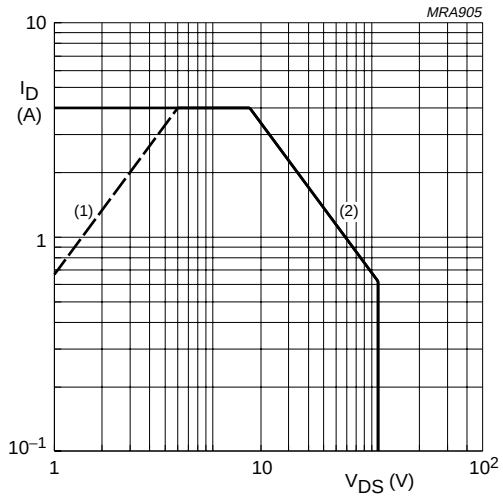
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	110	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	4	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	68	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

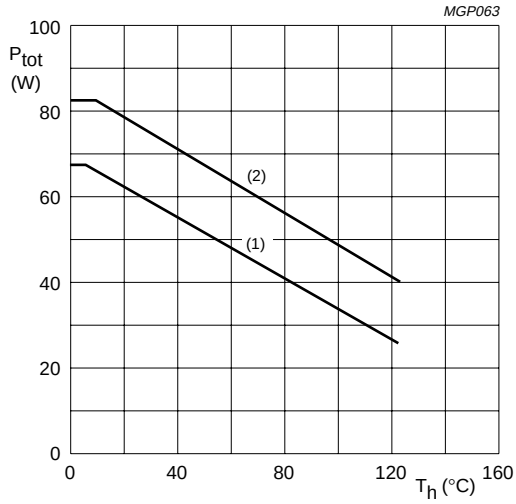
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 68 W	2.6 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	T_{mb} = 25 °C; P_{tot} = 68 W	0.3 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



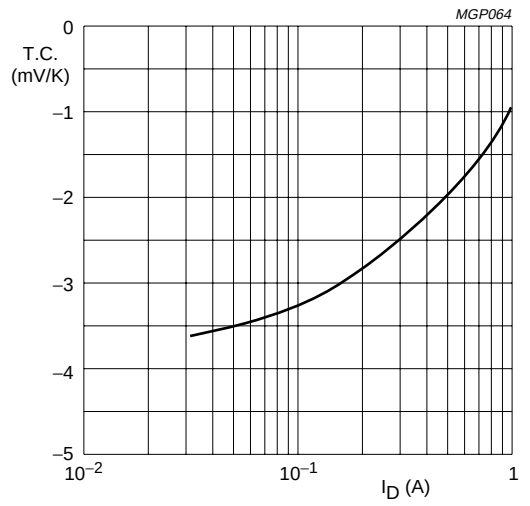
(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

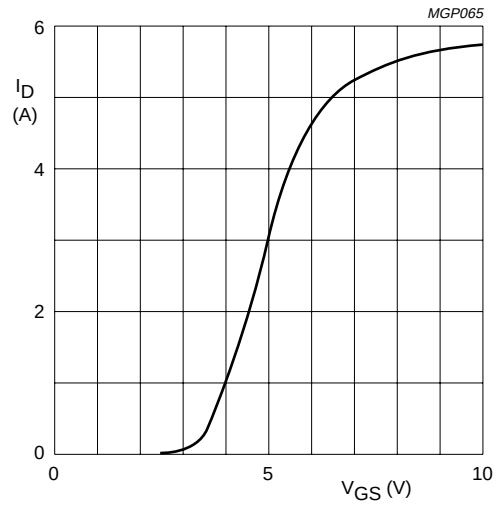
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 mA; V_{GS} = 0	110	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 50 V	–	–	100	μA
I_{GSS}	gate-source leakage current	±V_{GS} = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 10 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched pairs	I_D = 10 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 1 A; V_{DS} = 10 V	1.1	1.6	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 1 A; V_{GS} = 10 V	–	0.75	1.5	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	5.5	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	130	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	36	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	3.7	–	pF



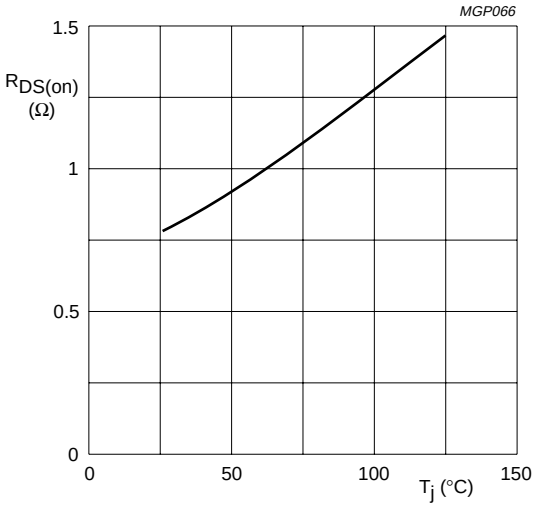
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



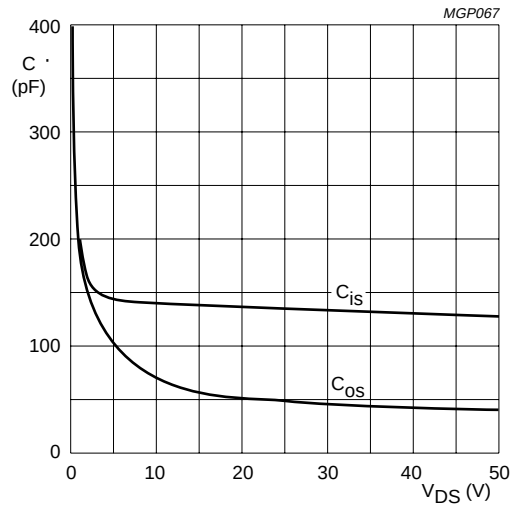
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.



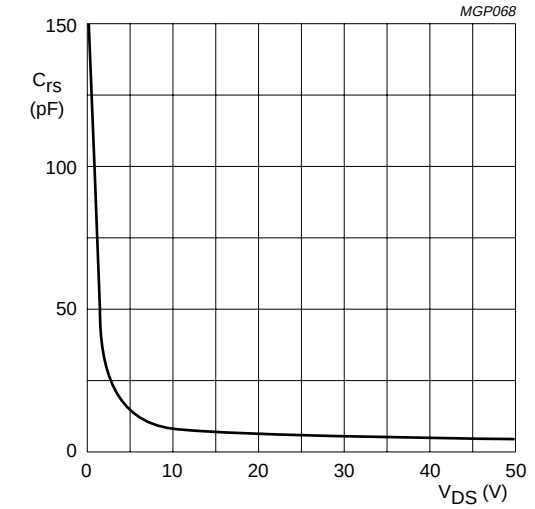
I_D = 1 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

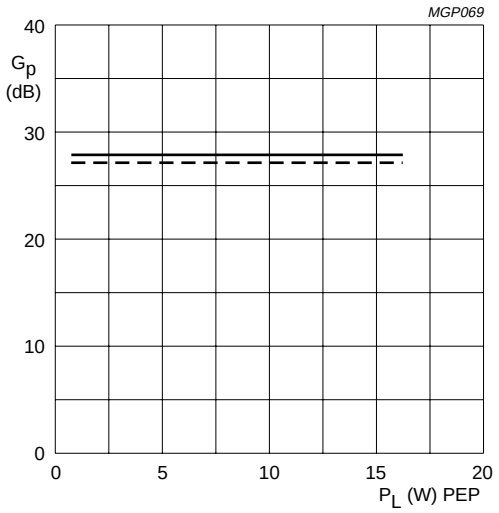
APPLICATION INFORMATION FOR CLASS-A OPERATION

T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W; unless otherwise specified.
RF performance in SSB operation in a common source circuit.
f_1 = 28.000 MHz; f_2 = 28.001 MHz.

P_L (W)	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	G_P (dB)	d_3 (dB) (note 1)	d_5 (dB) (note 1)	R_{GS} (Ω)
0 to 8 (PEP)	28	50	800	> 24 typ. 28	> –40 typ. –44	< –40 typ. –64	24 24

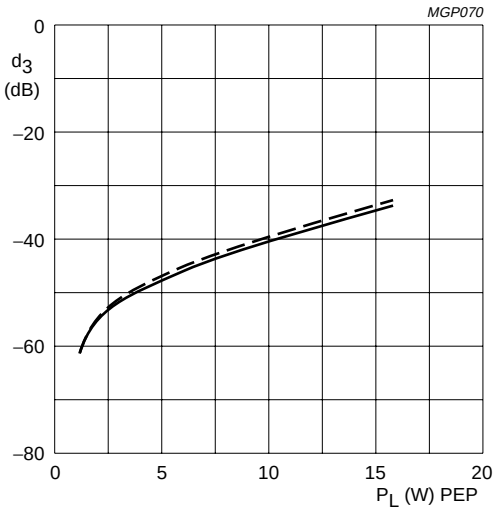
Note

1. Stated figures are maximum values encountered at any driving level between the specified value of PEP and are referred to the according level of either the equal amplified tones. Related to the according peak envelope power these figures should be decreased by 6 dB.



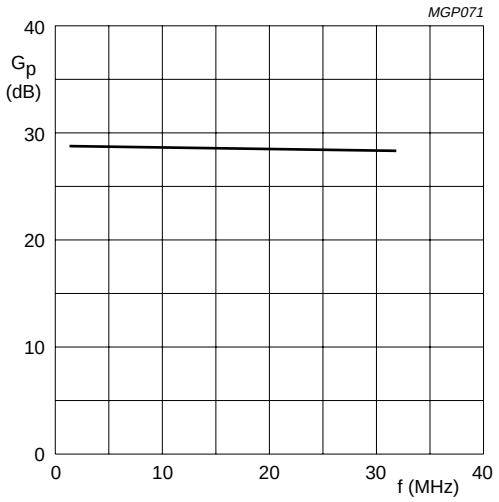
Class-A operation; V_{DS} = 50 V; I_{DQ} = 0.8 A;
R_{GS} = 24 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.9 Power gain as a function of load power, typical values.



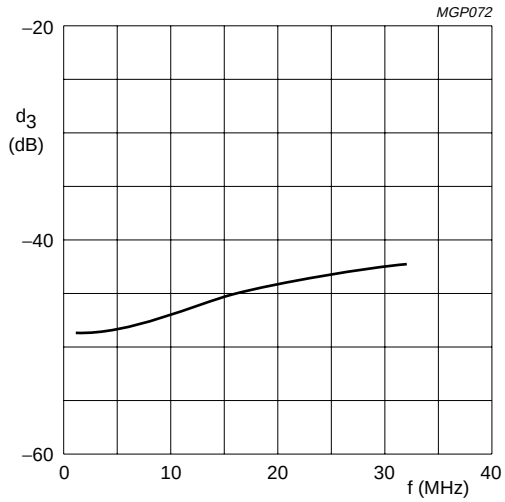
Class-A operation; V_{DS} = 50 V; I_{DQ} = 0.8 A;
R_{GS} = 24 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.10 Third order intermodulation distortion as a function of load power, typical values.



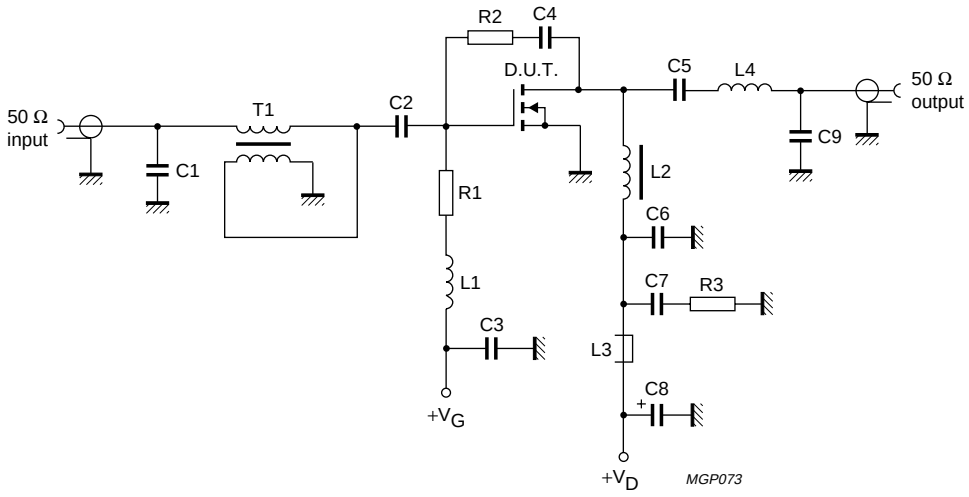
Class-A operation; V_{DS} = 50 V; I_{DQ} = 0.8 A;
P_L = 8 W (PEP); R_{GS} = 24 Ω; $f_1 - f_2$ = 1 MHz.

Fig.11 Power gain as a function of frequency, typical values.



Class-A operation; V_{DS} = 50 V; I_{DQ} = 0.8 A;
P_L = 8 W (PEP); R_{GS} = 24 Ω; $f_1 - f_2$ = 1 MHz.

Fig.12 Third order intermodulation distortion as a function of frequency, typical values.



f = 28 MHz.

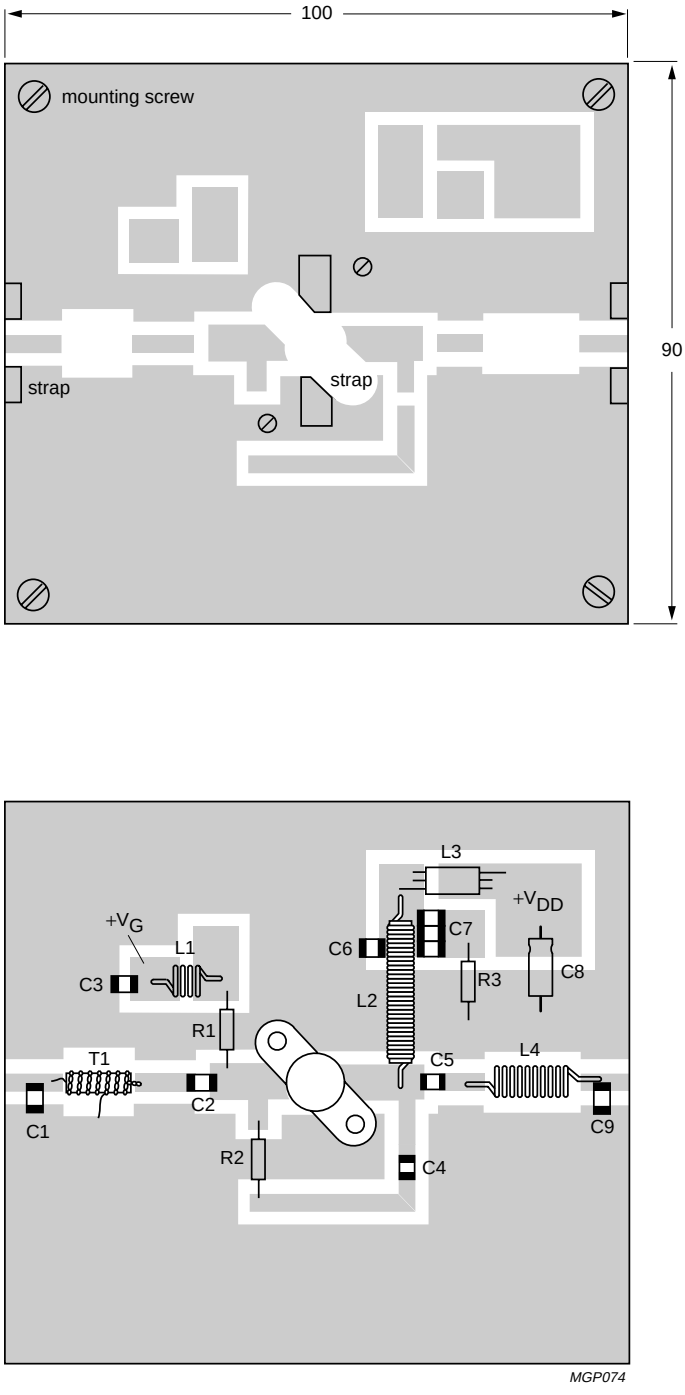
Fig.13 Test circuit for class-A operation.

List of components (class-A test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1	multilayer ceramic chip capacitor (note 1)	39 pF		
C2	multilayer ceramic chip capacitor	3 × 10 nF		2222 852 47103
C3, C4, C6	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C5	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C7	multilayer ceramic chip capacitor	3 × 100 nF		2222 852 47104
C8	aluminium electrolytic capacitor	10 μF, 63 V		2222 030 28109
C9	multilayer ceramic chip capacitor (note 1)	24 pF		
L1	4 turns enamelled 0.6 mm copper wire	86 nH	length 3.3 mm; int. dia. 5 mm; leads 2 x 2 mm	
L2	36 turns enamelled 0.7 mm copper wire wound on a rod grade 4B1 Ferroxcube drain choke	20 μH	length 30 mm; int. dia. 5 mm	4330 030 30031
L3	grade 3B Ferroxcube wideband RF choke			4312 020 36640
L4	8 turns enamelled 1 mm copper wire	189 nH	length 9.5 mm; int. dia. 5 mm; leads 2 x 3 mm	
R1	0.4 W metal film resistor	24 Ω		
R2	0.4 W metal film resistor	1500 Ω		
R3	0.4 W metal film resistor	10 Ω		
T1	4 : 1 transformer; 18 turns twisted pair of 0.25 mm copper wire with 10 twists per cm, wound on a grade 4C6 toroidal core		dimensions 9 x 6 x 3 mm	4322 020 97171

Note

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.



Note: The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets and straps at the two edges and under the source contacts.

Fig.14 Component layout for 28 MHz class-A test circuit.

APPLICATION INFORMATION FOR CLASS-AB OPERATION

T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W; unless otherwise specified.
RF performance in SSB operation in a common source circuit.
f_1 = 28.000 MHz; f_2 = 28.001 MHz.

P_L (W)	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	G_P (dB)	η_D (%)	d_3 (dB) (note 1)	d_5 (dB) (note 1)	R_{GS} (Ω)
30 (PEP)	28	50	150	typ. 24	typ. 40 (note 2)	typ. –35	typ. –40	22

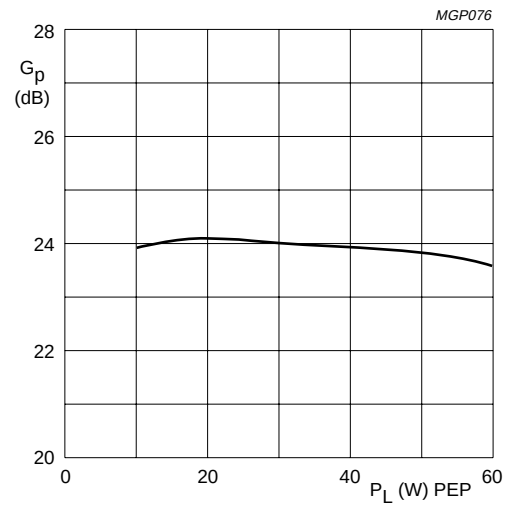
Notes

1. Stated figures are maximum values encountered at any driving level between the specified value of PEP and are referred to the according level of either the equal amplified tones. Related to the according peak envelope power these figures should be decreased by 6 dB.
2. 2-tone efficiency.

Ruggedness in class-AB operation

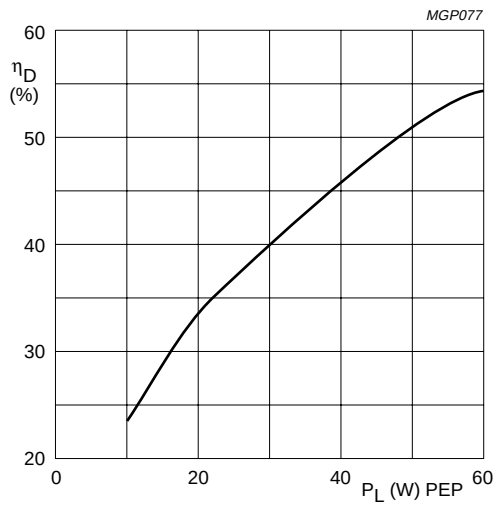
The BLF175 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases at P_L = 30 W single tone under the following conditions:

V_{DS} = 50 V; f = 28 MHz.



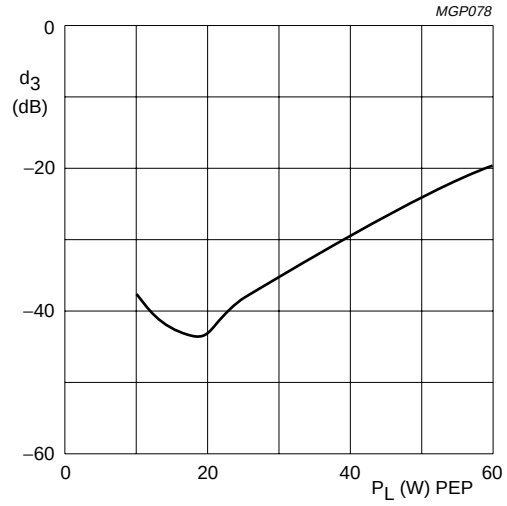
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A;
R_{GS} = 22 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.15 Power gain as a function of load power, typical values.



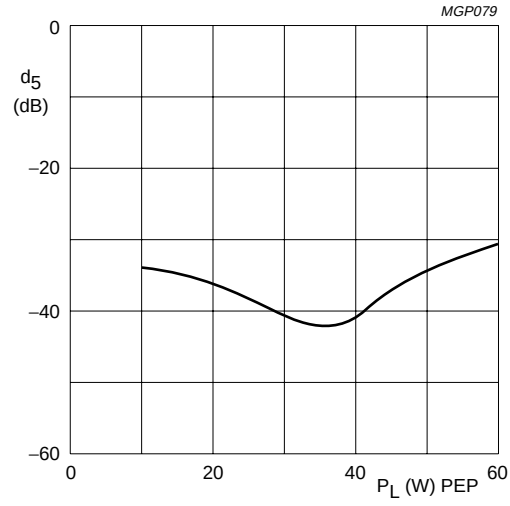
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A;
R_{GS} = 22 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.16 Two tone efficiency as a function of load power, typical values.



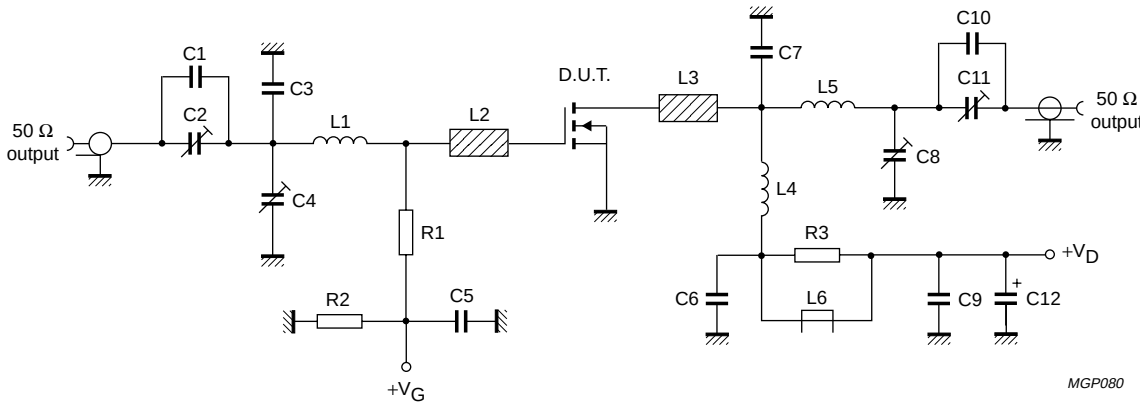
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A;
R_{GS} = 22 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.17 Third order intermodulation distortion as a function of load power, typical values.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A;
R_{GS} = 22 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.18 Fifth order intermodulation distortion as a function of load power, typical values.



f = 28 MHz.

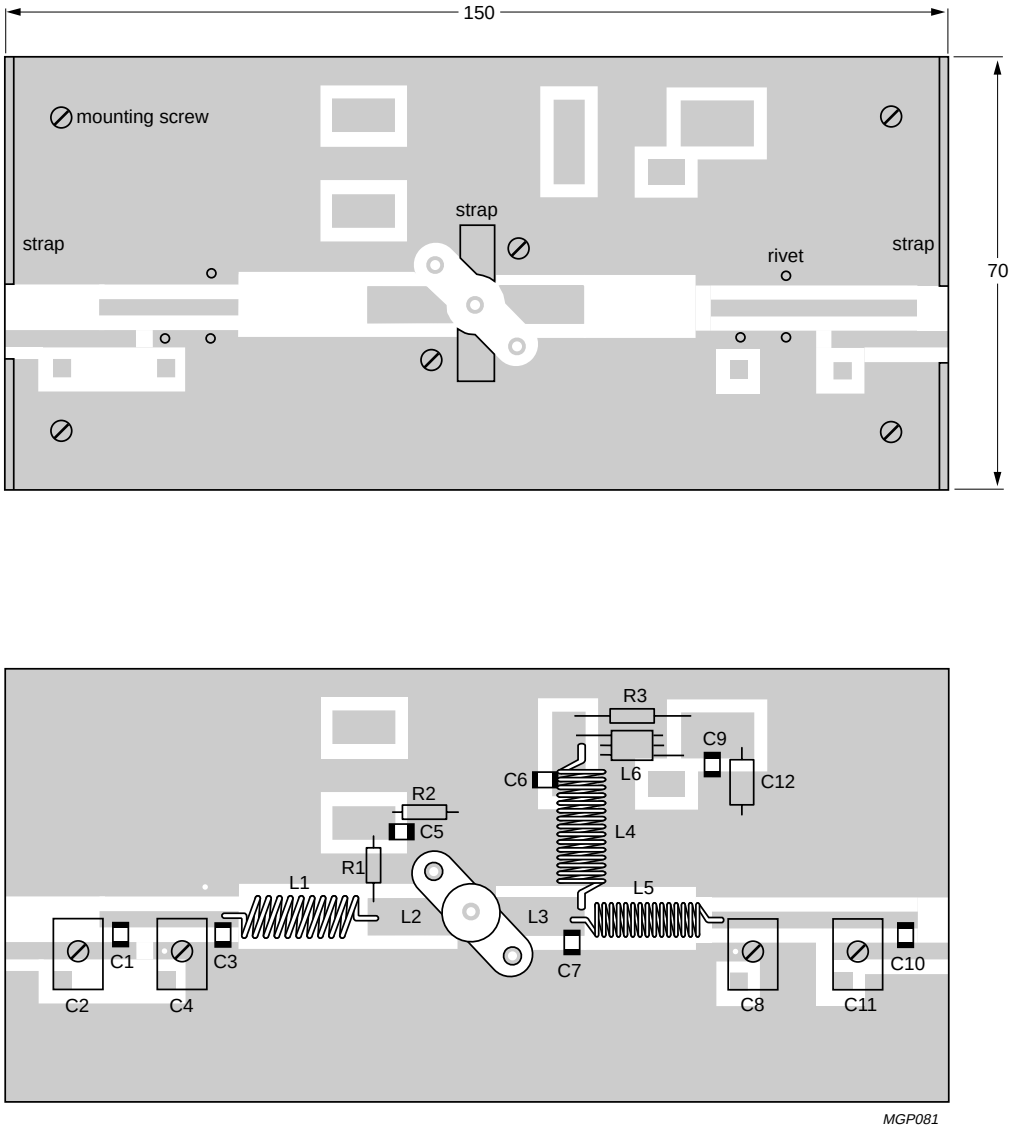
Fig.19 Test circuit for class-AB operation.

List of components (class-AB test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C10	multilayer ceramic chip capacitor (note 1)	62 pF		
C2, C4, C8, C11	film dielectric trimmer	5 to 60 pF		2222 809 07011
C3	multilayer ceramic chip capacitor (note 1)	51 pF		
C5, C6, C9	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C7	multilayer ceramic chip capacitor (note 1)	10 pF		
C12	aluminium electrolytic capacitor	10 μF, 63 V		2222 030 28109
L1	9 turns enamelled 1 mm copper wire	280 nH	length 11 mm; int. dia. 6 mm; leads 2 x 4 mm	
L2, L3	stripline (note 2)	30 Ω	length 10 mm; width 6 mm	
L4	14 turns enamelled 1 mm copper wire	1650 nH	length 20 mm; int. dia. 12 mm; leads 2 x 2 mm	
L5	10 turns enamelled 1 mm copper wire	380 nH	length 13 mm; int. dia. 7 mm; leads 2 x 3 mm	
L6	grade 3B Ferroxcube wideband RF choke			4312 020 36640
R1	0.4 W metal film resistor	22 Ω		
R2	0.4 W metal film resistor	1 MΩ		
R3	0.4 W metal film resistor	10 Ω		

Notes

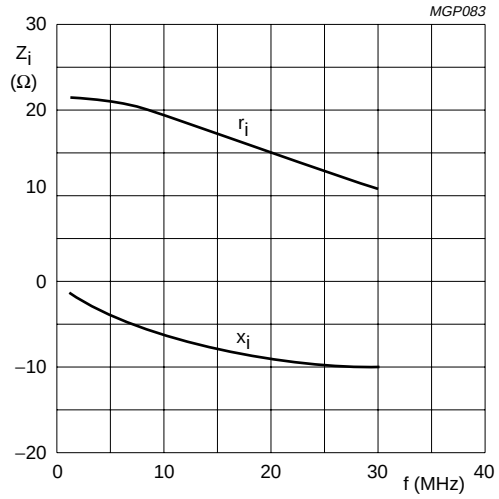
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ε_r = 4.5), thickness 1.6 mm.



Note: The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets and straps at the two edges and under the source contacts.

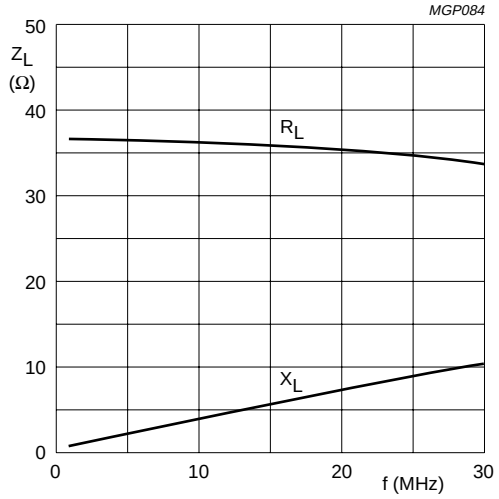
Dimensions in mm.

Fig.20 Component layout for 28 MHz class-AB test circuit.



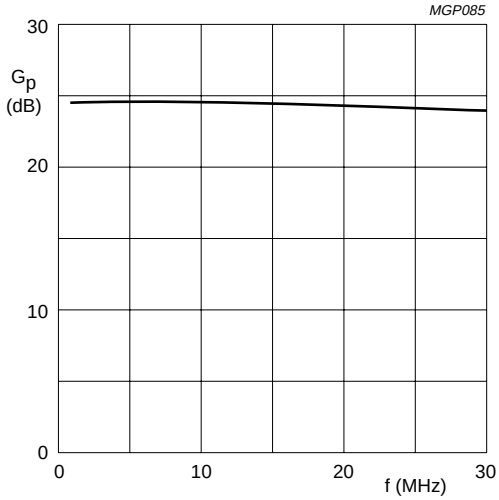
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A;
P_L = 30 W (PEP); R_{GS} = 22 Ω.

Fig.21 Input impedance as a function of frequency (series components), typical values.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A;
P_L = 30 W (PEP); R_{GS} = 22 Ω.

Fig.22 Load impedance as a function of frequency (series components), typical values.



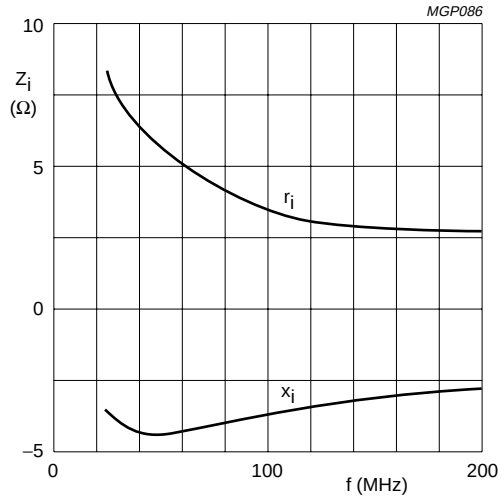
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A;
P_L = 30 W (PEP); R_{GS} = 22 Ω.

Fig.23 Power gain as a function of frequency, typical values.

APPLICATION INFORMATION FOR CLASS-AB OPERATION

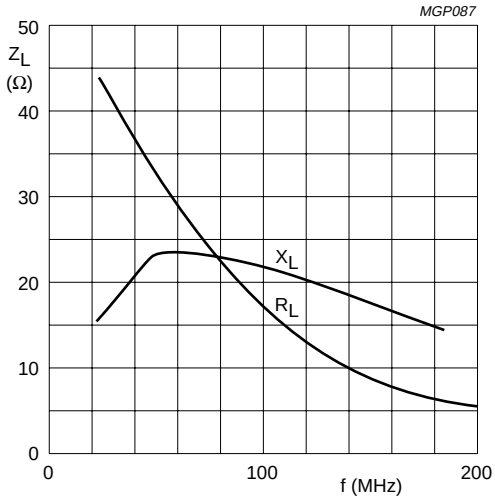
RF performance in SSB operation in a common source circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_P (dB)	η_D (%)	R_{GS} (Ω)
CW, class-B	108	50	30	30	typ. 20	typ. 65	10



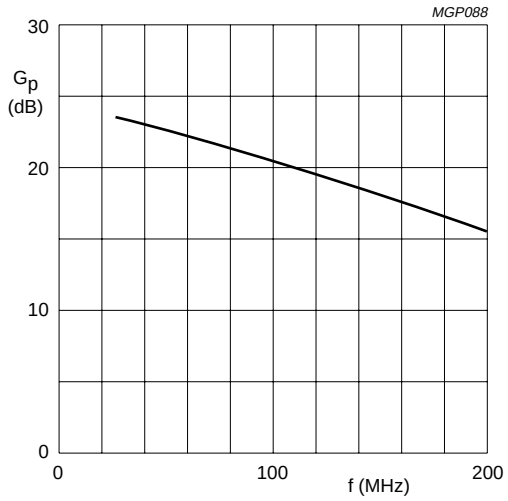
Class-B operation; V_{DS} = 50 V; I_{DQ} = 30 mA;
P_L = 30 W; R_{GS} = 10 Ω.

Fig.24 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 30 mA;
P_L = 30 W; R_{GS} = 10 Ω.

Fig.25 Load impedance as a function of frequency (series components), typical values.

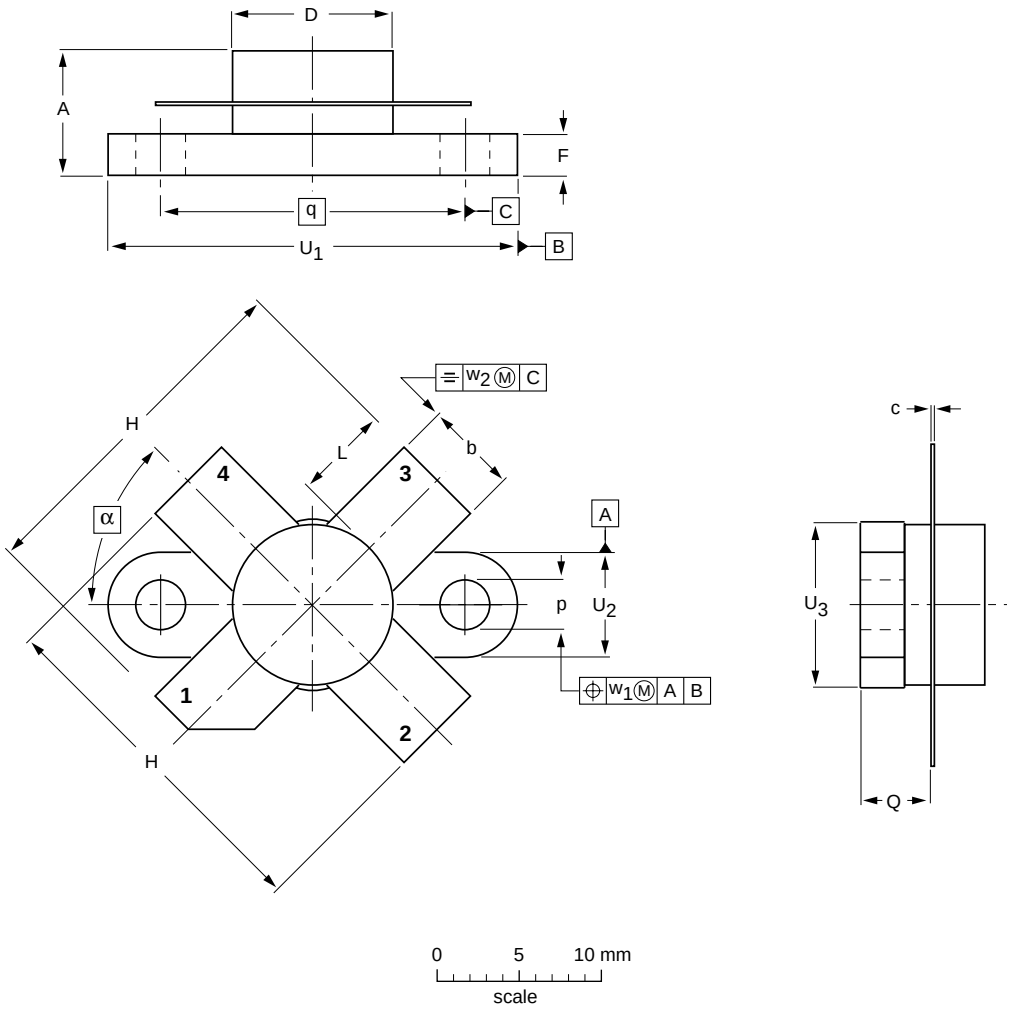


Class-B operation; V_{DS} = 50 V; I_{DQ} = 30 mA;
P_L = 30 W; R_{GS} = 10 Ω.

Fig.26 Power gain as a function of frequency, typical values.

PACKAGE OUTLINE

Flanged ceramic package; 2 mounting holes; 4 leads **SOT123A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	F	H	L	p	Q	q	U_1	U_2	U_3	w_1	w_2	α
mm	7.47 6.37	5.82 5.56	0.18 0.10	9.73 9.47	9.63 9.42	2.72 2.31	20.71 19.93	5.61 5.16	3.33 3.04	4.63 4.11	18.42	25.15 24.38	6.61 6.09	9.78 9.39	0.51	1.02	45°
inches	0.294 0.251	0.229 0.219	0.007 0.004	0.383 0.373	0.397 0.371	0.107 0.091	0.815 0.785	0.221 0.203	0.131 0.120	0.182 0.162	0.725	0.99 0.96	0.26 0.24	0.385 0.370	0.02	0.04	

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT123A						97-06-28

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.